WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a plurality of pages storing data;

a page buffer temporarily storing data by the page;

a correction circuit for correct a bit error of source data of a specific one of the pages;

a transferring circuit configured to provide the source data to the correction circuit and to provide amended data to the page buffer from the correction circuit; and

a replicating circuit configured to copy the source data into the page buffer and to store the amended data into another page from the page buffer.

2. The nonvolatile memory of claim 1, wherein the source data contains old parities.

3. The nonvolatile memory of claim 2, wherein the correction circuit generates new parities from the source data, and compares the new parities with the old parities.

4. The nonvolatile memory of claim 3, wherein the correction circuit comprises a circuit for generating column parities for bits composing one byte of the source data; and a circuit for generating line parities for bytes of the source data.

5. The nonvolatile memory of claim 1, wherein the nonvolatile memory is a NAND flash memory.

6. A nonvolatile memory comprising:

a data field composed of a plurality of pages for storing data;

a first storage configured to store first parities in a predetermined region of the data field, the first parities being generated during a programming operation for the page;

a page buffer for temporarily storing data by the page;

a moving circuit configured to copy source data stored in a specific one of the pages into the page buffer;

a parity circuit configured to generate second parities from the source data stored in the page buffer; and

a transfer circuit configured to transfer modified data of the source data to the page buffer in response to a result of comparing the first parities with the second parities.

7. The nonvolatile memory of claim 6, further comprising a second storage configured to store the amended data held in the page buffer into another page of the pages.

8. The nonvolatile memory of claim 6, wherein the second parities comprise column parities and line parities.

9. The nonvolatile memory of claim 8, wherein the parity circuit comprises a circuit for generating column parities for bits composing one byte of the source data; and a circuit for generating line parities for bytes of the source data.

10. The nonvolatile memory of claim 6, wherein the nonvolatile memory is a NAND flash memory.

11. A method of transferring source data of a specific page to another page in a nonvolatile memory having a page buffer structured to temporarily store data by the page, the source data containing old parities, the method comprising:

storing the source data into the page buffer;

generating new parities from the source data stored in the page buffer;

comparing the old parities with the new parities;

creating modified data from the source data in response to a result of the comparing; and

moving the modified data to the another page through the page buffer.

12. The method of claim 11, further comprising storing the old parities of the source data into a predetermined field of the memory before storing the source data into the page buffer.

13. The method of claim 11, further comprising informing an error status by the comparing result of the outside of the memory.

14. A nonvolatile memory comprising:

a data storage field composed of a plurality of pages storing data;

a page buffer for storing data of a specific one of the pages, being connected to the data storage field; and

an error correction circuit connected to the page buffer and including: a bit error detection circuit configured to detect a bit error of the data of the specific page; and a bit error correction circuit configured to amend the bit error.

15. The nonvolatile memory of claim 14, wherein the bit error detection circuit comprises:

a parity generator for creating new parities from the data stored in the page buffer; and

a comparator for generating error address information by comparing the new parities with old parities of the data.

16. The nonvolatile memory of claim 15, wherein the error address information is referred by the bit error correction circuit to correct the data and to transfer amended data to the page buffer.

17. The nonvolatile memory of claim 16, wherein the transfer of the amended data is managed by control signals.

18. The nonvolatile memory of claim 17, wherein the amended data are transcribed into the specific page and another page.

19. The nonvolatile memory of claim 14, wherein the nonvolatile memory is a NAND flash memory.